The effects of hydroxyl-free polystyrene buffer layer on electrical performance of pentacene-based thin-film transistors with high-k oxide gate dielectric

Aifang Yu, Qiong Qi, Peng Jiang, Chao Jiang

National Center for Nanoscience and Technology, No. 11, Beiyitiao Zhongguancun, Beijing 100190, China

Abstract

We have investigated the effects of hydroxyl-free polystyrene (PS) as buffer layer on pentacene-based low-voltage organic thin-film transistors (OTFTs). The PS buffer layer is formed on the HfO2 layer evaporated on Si substrate by spin-coating method prior to pentacene deposition, existence of which results in a dramatic increase of field effect mobility from 0.09 to 0.59 cm2/Vs and negligible hysteresis. The improved mobility and hysteresis of the OTFTs can be attributed to the formation of smooth and nonpolar hydroxyl-free PS/HfO2 gate dielectric surface. The PS insulator buffer layer can also effectively reduce gate leakage current by more than 70%. The results demonstrate that using appropriate polymer buffer layer is favorable to improve the performance of the OTFTs operating at low voltages with high mobility and good electrical stability.

1. Introduction

In recent years, organic thin-film transistors (OTFTs) have been the hot research topic due to their potential as low cost alternatives to amorphous silicon thin-film transistors and other simple Si-based electronic devices [1–3]. Although there have been significant advances in fabricating OTFTs with reasonably high electron and hole mobility, their generally high operating voltages still refrain it from many practical applications. To date, many high-k oxide gate dielectrics have been used to realize OTFTs with low operating voltage, including BST, Ta2O5, Al2O3, etc., which have reduced the operate voltage to 5 V [4–6].

However, these high-k oxides generally contain a high density of hydroxyl (–OH) groups on their top surface, and are characterized by a relatively rough surface morphology. The –OH groups and the rough surfaces result in an inferior channel/dielectric interface along with poor crystalline growth of the pentacene channel, and thus OTFTs fabricated on such dielectric surfaces usually exhibit undesirable device characteristics, including poor mobility, instability and large gate leakage current.

A thin low-k polymeric buffer layer has been demonstrated as a simple and effective way to modify the surface properties of a high-k dielectric surface, which retains the advantages from the both organic and inorganic dielectrics [7–9]. The charge carrier mobility of OTFT devices with low-k organic/high-k inorganic bilayer has been shown to be comparable to those of amorphous silicon transistor. However, a significant hysteresis in the electrical transfer characteristics was observed when using contained –OH group poly(vinylpenol)(PVP) or poly(vinylacohol) (PVA) as the buffer layer [7,10]. It has recently been reported that the hysteresis is mainly caused by the existence of hydroxyl groups from the polymer [11–14]. The –OH groups not only might cause remnant dipoles during the off-to-on gate swing, but also interact with diffusing water molecules and further create both donor and acceptor-like traps. Therefore, an appropriate polymer buffer layer is required in order to obtain high electrical performance and stable operation of the OTFTs.

In this work, we have used OH-free polystyrene (PS) as a buffer layer to optimize interface characteristics and minimize the leakage current. The PS is stable in air and can easily form uniform thin-films from solution by spin-coating. Because it does not have –OH groups in its chemical structure, crosslinks are not needed. A layer of high-k HfO2 acted as gate dielectric for construction of pentacene-based OTFTs to decrease operating voltage. The inorganic dielectric layer was fabricated by ion-beam-assisted deposition (IBAD) technique at room temperature. The effects of hydroxyl-free PS as buffer layer on electrical performance of OTFTs with high-k HfO2 gate dielectric were explored and discussed.

2. Experiment details

A typical of device was fabricated by using a piece of heavily doped Si-n++ wafer as the substrate and gate electrode. Prior to the deposition of the gate-dielectric layer, the substrate was...
cleaned with acetone, ethanol, and deionized water in that order. A layer of about 300 nm thick HfO$_2$ film was deposited on the substrate by an IBAD process at room temperature. During the deposition process, the base pressure of the deposition chamber was $2 \times 10^{-3}$ Pa, which increased to $1 \times 10^{-2}$ Pa when Ar and O$_2$ flowed into the ion source. For the preparation of PS buffer layer, a 0.5 wt.% solution of PS (Alfa Aesar, M.W.100,000) in toluene was applied by spin coating and cured for 7 h at 70 $^\circ$C in a vacuum oven to remove residual solvent. The final thickness of the PS film was approximately 25 nm, as measured by the surface profiler. Pentacene (purchased from Aldrich) without any further purification was thermally sublimed onto the PS/HfO$_2$ and HfO$_2$ gate dielectric at the same run with a growth rate of 2.1 nm/min up to 50 nm thickness at room temperature. Finally, source/drain Au electrodes were patterned through a shadow mask, yielding bottom gate and top contact OTFT structure. The channel width and length were 2000 $\mu$m and 50 $\mu$m, respectively. Capacitance structures of Au/HfO$_2$/Si and Au/PS/HfO$_2$/Si were also processed to determine the actual capacitance of the gate dielectric at a high frequency (1 MHz) using Keithley 590 CV analyzer system. Atomic force microscopic (AFM) images including root-mean-square roughness ($R_{rms}$) were obtained in a tapping mode. All I–V electrical characteristics of the current–voltage ($I_{DS}$–$V_{DS}$) of the OTFT device with the PS buffer layer significantly increases to 250 nA to 75 nA. This indicates that the PS insulator buffer layer contributes to the decrease of the leakage current in OTFTs. The induced charge may be prohibited from penetrating through the gate insulator layer above the gate oxide. The negligible hysteresis observed for the PS-modified OTFT displays negligible hysteresis, while the OTFT only with HfO$_2$ as gate dielectric shows some hysteresis between the forward and reverse traces.

### 3. Results and discussions

**Fig. 1.** Output characteristics of pentacene TFTs fabricated on (a) HfO$_2$ gate dielectric and (b) PS-modified HfO$_2$ gate dielectric.

**Fig. 2.** Transfer characteristics of pentacene TFTs fabricated on (a) HfO$_2$ gate dielectric and (b) PS-modified HfO$_2$ gate dielectric. The arrows indicate the direction of the $V_{GS}$ sweep at $V_{DS} = -5$ V.

Distortion of the $I_{DS}$–$V_{DS}$ curves in the linear region can be clearly seen because of the $I_{DS}$ offset when $V_{DS} = 0$ V. The increase of positive current in the near 0 V $V_{DS}$ region with enhancement of $V_{GS}$ is mainly due to the leakage current through the gate insulator layer between source/drain and gate electrodes. In contrast, OTFTs with the PS-modified HfO$_2$ as a gate dielectric exhibit excellent output curves without obvious current leakage, as shown in Fig. 1b.

Here $C_i$ is the capacitance per unit area of the gate insulator and $V_T$ is the threshold voltage. The obtained electric parameters are summarized in Table 1. As we can see, insertion of the PS into the OTFT results in a drastic enhancement in the field effect mobility from 0.09 to 0.59 cm$^2$/Vs. To further confirm the electrical stability of the OTFTs, we have detected the hysteresis behavior of the current–voltage ($I–V$) curves. It can be seen that the PS-modified OTFT displays negligible hysteresis, while the OTFT only with HfO$_2$ as gate dielectric shows some hysteresis between the forward and reverse traces. The negligible hysteresis observed for the PS-modified dielectrics reveals the very low activation and deactivation rates of traps at the PS/pentacene interface.
Table 1
Electrical parameters of transistors based on HfO2- and PS-modified HfO2 gate dielectric.

<table>
<thead>
<tr>
<th>Gate dielectric</th>
<th>Contact angle (°) water</th>
<th>Mobility (cm²/Vs)</th>
<th>Gate leakage (nA)</th>
<th>Capacitance (nF/cm²)</th>
<th>Threshold voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HfO2</td>
<td>80</td>
<td>0.09</td>
<td>250</td>
<td>64</td>
<td>−1.62</td>
</tr>
<tr>
<td>HfO2/PS</td>
<td>96</td>
<td>0.59</td>
<td>75</td>
<td>42</td>
<td>−2</td>
</tr>
</tbody>
</table>

Fig. 3. Gate leakage current vs. \(V_{DS}\) at \(V_{GS} = −3\) and \(−5\) V.

slightly changed. The capacitances of HfO2 and HfO2/PS were 64 and 42 nF/cm², respectively.

It is widely believed that the performance of OTFTs highly depends on the quality of the dielectric/channel interface because the carrier is confined within a very short distance from that interface. The PS buffer layer improves the surface quality of the HfO2 gate insulator and optimizes the growth behavior of the pentacene film. This can be demonstrated in Fig. 4. It is noted that the \(R_{rms}\) reduces from 0.9 nm to 0.3 nm and the surface becomes more hydrophobic after PS treatment which is illustrated as the change of contact angles. Correspondingly, the pentacene film exhibits well-formed terraces and large grains when grown on PS-modified HfO2 gate dielectric. The average grain size is about 1.0 μm. Similar morphology for pentacene film has been reported by Yoon [7]. On the contrary, the pentacene film on HfO2 shows much smaller grains with average size 200 nm. Our result is consistent with the common view that the field effect mobility is increased with increased pentacene grain sizes [9,16]. Smooth and more hydrophobic surface after PS treatment is in favor of the growth of pentacene thin-film and low density chemical defects at the interface, which minimizes carrier trap at grain boundaries and at the interface between insulator/organic semiconductor for better carriers transportation. This is useful to obtain greater saturation current and higher field effect mobility.

Im and co-workers [12] have integrated hysteresis to three general mechanisms: (1) channel/dielectric interface induced effect; (2) residual dipole-induced effect; (3) the effects of charges injected from gate electrode. In our case, judging by the hysteresis direction, as shown in Fig. 2a, −OH groups at the pentacene/HfO2 interface might be responsible for the hysteresis observed in our OTFTs because they are the sites for electron trapping. It is very similar to that observed by using SiO2 as gate dielectric [11,17,18]. Therefore,

Fig. 4. The AFM images of (a) HfO2, and (b) HfO2 that was modified with PS. The AFM images in (c) and (d) show the morphologies of the pentacene films corresponding to (a), and (b), respectively. The scanned area is 5 μm × 5 μm. Insets in (a) and (b) are images of water drops on gate dielectric for contact angle measurement.
negligible hysteresis found in our experiments might suggest that the PS layer has effectively modified HfO$_2$ interface by C$_6$H$_5$– groups instead of –OH groups, which could induce a more hydrophobic interface and further avoid new traps. As a comparison, in the case of PVP or PVA used as a buffer layer, it is difficult to completely remove all –OH in the polymer layer even if –OH groups are substituted by crosslink agents. The absorbed water and residual –OH groups in the polymer can act as trapping sites, and then generate new hysteresis. Water molecules might migrate into the channel region through the grain boundaries, where they create both donor- and acceptor-like traps, leading to significant hysteresis and degradation of device performance [16,19]. On the other hand, the PS used in our device does not bear –OH groups in its chemical structure. Thus, this is unfavorable for adsorption of water into the buffer polymer layer [20]. Moreover, large dendritic pentacene grains can be formed on the PS-modified HfO$_2$ gate dielectric due to the existence of PS layer. It reduces the number of grain boundaries and benefits to the decrease of the hysteresis behavior. Therefore, PS buffer layer plays an important role in elimination of hysteresis. It was our next studying target to further clarify the origin of traps occurred at the interface between the gate-dielectric layer and the pentacene layer.

4. Conclusions

In conclusion, pentacene-based organic thin-film transistors with HfO$_2$- or PS-modified HfO$_2$ gate insulator have been constructed on heavily doped Si substrates and their electrical performance was investigated. The OTFTs with the PS-modified HfO$_2$ insulator layer show offset-free $I_{DS}$, drastic field effect mobility enhancement and negligible hysteresis in contrast to the OTFTs without PS modification. Improved pentacene growth and the formation of nonpolar OH-free groups on smooth PS/HfO$_2$ surface contribute to the improved device performance. Our design in PS-modified HfO$_2$ gate insulator provides a new opportunity in the optimization of the OTFTs operating at low voltages with low gate leakage current, high mobility, and good electrical stability.

References